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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,330	08/17/2001	Jon M. Huppenthal	SRC012	4801

25235 7590 12/03/2004

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EXAMINER
NGUYEN, TRONG NHAN P

ART UNIT	PAPER NUMBER
2152	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,330	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Jack P Nguyen	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *37-51* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-51 are being examined.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Group 1: Claims 1-36 are drawn to a method for enhancing data transfer rates for clustered computers via shared memory in 709, subclass 213.

II. Group 2: Claims 37-51 are drawn to a method for connecting array processor element to perform data translations using computer algorithms in class 712, subclass 11.

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. Invention I has a separate utility such as in a system lacking connecting array processor element to perform data translations using computer algorithms. Invention II has a separate utility such as in a system lacking for enhancing data transfer rates for clustered computers via shared memory. See MPEP § 806.05(d).

These inventions are distinct for the reasons given above, and the search required for each Group is different and not co-extensive for examination purpose. For example, the searches for the two inventions would not be co-extensive because these groups would require different searches on PTO's classification class and subclass as following:

(a) Group I search (claims 1-36) would require use of search **Class 709, subclass 213.**

(b) Group II search (claims 37-51) would require use of search **Class 712, subclass 11**.

A telephone call was conducted with Mr. William Kubida, the applicant's representative, on November 18, 2004 to address the possibility of a restriction election. The applicant elected Group I, without traverse.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claims 37-51 are withdrawn from consideration.

Claims 1-36 are now presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9, 10, and 36 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. The specification does not disclose the enablement for a processor comprises a plurality of processors, processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device and on said data connection from said external device prior to transmission to said controller on said memory module bus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al, 6,633,945 (Fu hereafter) in view of Scardamalia et al, 6,295,571 (Scardamalia hereafter).

As per claim 1, Fu teaches a computer system comprising: at least one processor (120, fig. 2); a controller (220, fig. 2) for coupling said at least one processor to a peripheral bus control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus (151, fig. 2; PCI bus allows plurality of peripherals to be connected); at least one memory module slot coupled to said memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory

module slot for providing a data connection to an external device coupled thereto. However, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu and Scardamalia to use a memory adapter module for providing data connection to external device to increase efficiency of transactions by reducing bottlenecks and delays in the memory connection fabric and the I/O channels as disclosed by Scardamalia in [col. 1, lines 63-65].

Claim 13 is rejected for similar reasons as claim 1 above. Fu further teaches alternative embodiments of the above invention by having a controller for coupling said at least one processor to a graphics control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one graphics bus connection coupled to said graphics control block by a graphics bus (154, fig. 2). at least one memory module slot coupled to said memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto. However, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu and Scardamalia to use a memory

adapter module for providing data connection to external device to increase efficiency of transactions by reducing bottlenecks and delays in the memory connection fabric and the I/O channels as disclosed by Scardamalia in [col. 1, lines 63-65].

As per claims 2-4, Fu teaches a control connection to said processor element coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said data connection to said processor element (see fig. 2; col. 3, lines 51-61); memory module bus comprises a DIMM bus (115, fig. 2, col. 3, line 45); processor element comprises a DIMM physical format for retention within said at least one memory module slot (col. 3, lines 45).

As per claims 5-6, in conjunction with claims 2-4, Fu teaches a DIMM memory module bus and processor element processor element comprises a DIMM physical format for retention within said at least one memory module slot as stated previously. Fu and Scardamalia do not explicitly disclose memory module bus comprises a RIMM bus and processor element comprises a RIMM physical format for retention within said at least one memory module slot. However, it would have been obvious to one of ordinary skill in the art to introduce a variation of the Fu and Scardamalia teachings by using equivalent functional memory formats such as RIMM technologies.

As per claims 7-8, Fu teaches external device comprises one of another computer system (fig. 13; *plurality of systems are interconnected to increase speed and performance*); peripheral bus comprises PCI bus (153, fig. 2).

As per claims 9-10, Fu teaches the memory interface element (3108, fig. 3) is operative to alter data received from said (transaction) controller (400, fig. 3) on said

memory module bus (115, fig. 3) prior to transmission on data to memory control unit (col. 5, lines 9-15). Fu does not explicitly disclose processor element (memory module) transmitting data to external device for processing. Scardamalia teaches the memory adapter module transmitting transaction requests to external device (100, fig. 1) for assistance in transactions processing (col. 5, lines 30-35). Hence, it would have been obvious to one of ordinary skill in the art to introduce a modification of the Scardamalia teachings by using external helpers (devices) to expedite transactions processing.

As per claim 11, Fu and Scardamalia do not explicitly disclose processor element comprises: a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection. However, it is well known and would have been obvious to one of ordinary skill in the art to use FPGA technology because FPGA provides an array of logic elements that are programmable and configurable based on the user's requirements.

As per claim 12, Fu teaches a system comprises a plurality of processors (120, fig. 2; CPU0, CPU1, CPU2, etc.) Fu and Scardamalia do not teach one processor comprises a plurality of processors. However, it is well known and would have been obvious to one of ordinary skill in the art to use a plurality of processors in a system to increase power and performance levels of the system.

Claims 14-16 are rejected for similar reasons as claims 2-4, 13 addressed above.

Claims 17-18 are rejected for similar reasons as claims 5-6 addressed above.

Claims 19-20 are rejected for similar reasons as claims 7-8 addressed above. Fu further teaches peripheral bus comprises an AGP bus (154, fig. 2).

Claims 21-22 are rejected for similar reasons as claims 9-10 addressed above.

Claims 23-24 are rejected for similar reasons as claims 11-12 addressed above.

Claims 25-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al, 6,633,945 (Fu hereafter) in view of Scardamalia et al, 6,295,571 (Scardamalia hereafter).

Claim 25 is rejected for similar reasons as claims 1 and 25 above. Fu further teaches alternative embodiments of the above invention by having a controller for coupling said at least one processor to a graphics control block (240, fig. 2) and a memory module bus (114, fig. 2); at least one graphics bus connection coupled to said graphics control block by a graphics bus (154, fig. 2). at least one memory module slot coupled to said memory module bus (1300, fig. 2, col. 3, lines 41-45; memory module slots allow plurality of DIMM chips to be coupled). Fu does not explicitly disclose a processor element associated with said at least one memory module slot for providing a data connection to an external device coupled thereto. However, Scardamalia discloses a memory adapter module (300, fig. 1) associated with at least one memory module slot for providing a data connection to an external device (100, fig. 1) coupled thereto (col. 5, lines 24-28). Hence, it would have been obvious to one of ordinary skill in the art to be motivated to combine and modify the teachings of Fu and Scardamalia to use a memory adapter module for providing data connection to external device to increase efficiency of transactions by reducing bottlenecks and delays in the memory connection fabric and the I/O channels as disclosed by Scardamalia in [col. 1, lines 63-

65]. Furthermore, Fu and Scardamalia do not explicitly teach a controller for coupling said at least one processor to a system maintenance control block and a memory module bus; at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus. However, it would have been obvious to one of ordinary skill in the art to introduce various embodiments of the Fu and Scardamalia teachings such as system maintenance control block and system maintenance bus connection as a design choice without departing from the spirit and scope of the invention as disclosed by Fu in [col. 8, lines 60-63].

Claims 26-28 are rejected for similar reasons as claims 2-4 and 25 addressed above.

Claims 29-30 are rejected for similar reasons as claims 5-6 addressed above.

Claims 31-32 are rejected for similar reasons as claims 7-8 addressed above. Fu further teaches peripheral bus comprises an AGP bus (154, fig. 2). Fu and Scardamalia do not explicitly disclose peripheral bus comprises an SM bus. However, as stated in claims 13 and 25 above, it would have been obvious to one of ordinary skill in the art to include still another embodiment of the Fu teachings to include SM bus as a design choice without departing from the spirit or scope of the invention.

Claims 33-34 are rejected for similar reasons as claims 9-10 addressed above.

Claims 35-36 are rejected for similar reasons as claims 11-12 addressed above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Dell et al, 6,108,730 ; Wallach et al, 6,202,111 ; Fischer, 4,783,730 ; Cloutier, 5,892,962 ; Shido et al, 5,230,057 ; DeHon et al, 6,052,773 ; Foster, 6,052,134 ; Bauman, 6,799,252 ; Archer et al, 6,148,356 ; Behrbaum et al, 6,326,973

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack P Nguyen whose telephone number is (571) 272-3945. The examiner can normally be reached on M-F 8:30-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jpn

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PRIMARY EXAMINER